ECE 485

Tomasulo's Algorithm

Architecture Assumptions

- Execution Stage:
  - Load: 2 cycle
  - Add/Sub: 3 cycles
  - Mul: 7 cycles
  - Div: 13 cycles

Clock Cycle: 1

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1		
LW	F2,44(R3)					
MULT	F0,F2,F4					
SUB	F8,F2,F6					
DIV	F10,F0,F6					

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1	Y	Load	R2				32 + R2
Load2							
Add1							
Add2							
Mult1							
Mult2							

Regs

F0	F2	F4	F6	F8	F10
			Load1		

Clock Cycle: 2

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 -	
LW	F2,44(R3)			2		
MULT	F0,F2,F4					
SUB	F8,F2,F6					
DIV	F10,F0,F6					

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1	Y	Load	R2				32 + R2
Load2	Y	Load	R3				44 + R3
Add1							
Add2							
Mult1							
Mult2							

Regs

F0	F2	F4	F6	F8	F10
	Load2		Load1		

Clock Cycle: 3

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 - 3	
LW	F2,44(R3)			2	3 -	
MULT	F0,F2,F4			3		
SUB	F8,F2,F6					
DIV	F10,F0,F6					

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1	Y	Load	R2				32 + R2
Load2	Y	Load	R3				44 + R3
Add1							
Add2							
Mult1	Y	Mul		F4	Load2		
Mult2							

Regs

F0	F2	F4	F6	F8	F10
Mult1	Load2		Load1		

Clock Cycle: 4

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 - 3	4
LW	F2,44(R3)			2	3 - 4	
MULT	F0,F2,F4			3	← stall	
SUB	F8,F2,F6			4		
DIV	F10,F0,F6					

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1							
Load2	Y	Load	R3				44 + R3
Add1	Y	Sub		M[32 + R2]	Load2		
Add2							
Mult1	Y	Mul		F4	Load2		
Mult2							

Regs

F0	F2	F4	F6	F8	F10
Mult1	Load2		M[32 + R2]	Add1	

Clock Cycle: 5

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 - 3	4
LW	F2,44(R3)			2	3 - 4	5
MULT	F0,F2,F4			3	← stall	
SUB	F8,F2,F6			4	← stall	
DIV	F10,F0,F6			5		

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1							
Load2							
Add1	Y	Sub	M[44 + R3]	M[32 + R2]			
Add2							
Mult1	Y	Mul	M[44 + R3]	F4			
Mult2	Y	Div		F6	Mult1		

Regs

F0	F2	F4	F6	F8	F10
Mult1	M[44 + R3]			Add1	Mult2

Clock Cycle: 6

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 - 3	4
LW	F2,44(R3)			2	3 - 4	5
MULT	F0,F2,F4			3	6 -	
SUB	F8,F2,F6			4	6 -	
DIV	F10,F0,F6			5	← stall	

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1							
Load2							
Add1	Y	Sub	M[44 + R3]	M[32 + R2]			
Add2							
Mult1	Y	Mul	M[44 + R3]	F4			
Mult2	Y	Div		F6	Mult1		

Regs

F0	F2	F4	F6	F8	F10
Mult1				Add1	Mult2

Clock Cycle: 8

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 - 3	4
LW	F2,44(R3)			2	3 - 4	5
MULT	F0,F2,F4			3	6 -	
SUB	F8,F2,F6			4	6 - 8	
DIV	F10,F0,F6			5	← stall	

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1							
Load2							
Add1	Y	Sub	M[44 + R3]	M[32 + R2]			
Add2							
Mult1	Y	Mul	M[44 + R3]	F4			
Mult2	Y	Div		F6	Mult1		

Regs

F0	F2	F4	F6	F8	F10
Mult1				Add1	Mult2

Clock Cycle: 9-11

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 - 3	4
LW	F2,44(R3)			2	3 - 4	5
MULT	F0,F2,F4			3	6 -	
SUB	F8,F2,F6			4	6 - 8	9
DIV	F10,F0,F6			5	← stall	

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1							
Load2							
Add1							
Add2							
Mult1	Y	Mul	M[44 + R3]	F4			
Mult2	Y	Div		F6	Mult1		

Regs

F0	F2	F4	F6	F8	F10
Mult1				~P~	Mult2

Clock Cycle: 12

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 - 3	4
LW	F2,44(R3)			2	3 - 4	5
MULT	F0,F2,F4			3	6 - 12	
SUB	F8,F2,F6			4	6 - 8	9
DIV	F10,F0,F6			5	← stall	

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1							
Load2							
Add1							
Add2							
Mult1	Y	Mul	M[44 + R3]	F4			
Mult2	Y	Div		F6	Mult1		

Regs

F0	F2	F4	F6	F8	F10
Mult1					Mult2

Clock Cycle: 13

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 - 3	4
LW	F2,44(R3)			2	3 - 4	5
MULT	F0,F2,F4			3	6 - 12	13
SUB	F8,F2,F6			4	6 - 8	9
DIV	F10,F0,F6			5	← stall	

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1							
Load2							
Add1							
Add2							
Mult1							
Mult2	Y	Div	~Q~	F6			

Regs

F0	F2	F4	F6	F8	F10
~Q~					Mult2

Clock Cycle: 26

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 - 3	4
LW	F2,44(R3)			2	3 - 4	5
MULT	F0,F2,F4			3	6 - 12	13
SUB	F8,F2,F6			4	6 - 8	9
DIV	F10,F0,F6			5	14 - 26	

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1							
Load2							
Add1							
Add2							
Mult1							
Mult2	Y	Div	~Q~	F6			

Regs

F0	F2	F4	F6	F8	F10
					Mult2

Clock Cycle: 27

Instruction Status

Instruction	dest	j	k	Issue	Execution Completed	Write Back
LW	F6,32(R2)			1	2 - 3	4
LW	F2,44(R3)			2	3 - 4	5
MULT	F0,F2,F4			3	6 - 12	13
SUB	F8,F2,F6			4	6 - 8	9
DIV	F10,F0,F6			5	14 - 26	27

Reservation Stations

Functional Unit	Busy	Op	Vj	Vk	Qj	Qk	A
Load1							
Load2							
Add1							
Add2							
Mult1							
Mult2							

Regs

F0	F2	F4	F6	F8	F10
					~R~